UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,094	11/06/2001	Shigeo Matsumoto	SONYJP 3.0-217	6045

530 7590 06/29/2004

LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK
600 SOUTH AVENUE WEST
WESTFIELD, NJ 07090

EXAMINER	
VU, PHUONG T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/993,094	MATSUMOTO ET AL.	
	Examiner	Art Unit	
	Phuong T. Vu	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Clayton et al. (US 6,665,190B2). Regarding claim 1, the reference discloses an integrated circuit device 10 adapted to be loaded in host equipment comprising a substantially rectangular main body unit 16, a first set of connection terminals 22 provided at one end of said main body unit to enable electrical connection between said main body unit and the host equipment, a plurality loading sections 28 provided in said main body unit, each of said loading sections having an insertion opening along an edge of said main body unit transverse to said one end and a second set of connection terminals 20 spaced from said insertion opening, a plurality of substantially rectangular integrated circuit chips 12 assembled in respective ones of said loading sections, each of said integrated circuit chips including a built-in integrated circuit unit forming a memory unit or a logic circuit and a third set of connection terminals 14 for establishing electrical connection between said second set of connection terminals in said loading

section and said integrated circuit unit, a guide support provided in each of said loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of said integrated circuit chips into said loading sections and a controller disposed in said main body unit for controlling the writing of information signals to and the readout of information signals from said plurality of integrated circuit chips loaded in said loading sections.

Regarding claim 2, the reference discloses a memory device 10 adapted to be loaded in host equipment comprising a substantially rectangular main body unit 16, a first set of connection terminals 22 provided at one end of said main body unit to enable electrical connection between said main body unit and the host equipment, a plurality loading sections 28 provided in said main body unit, each of said loading sections having an insertion opening along an edge of said main body unit transverse to said one end and a second set of connection terminals 20 spaced from said insertion opening, a plurality of substantially rectangular memory chips 12 including a memory unit therein and a third set of connection terminals 14 for establishing electrical connection between said second set of connection terminals in said loading section and said memory unit, a guide support provided in each of said loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of said integrated circuit chips into said loading sections and a controller disposed in said main body unit for controlling the writing of information signals to and the readout of information signals from said plurality of integrated circuit chips loaded in said loading sections.

Regarding claim 3, it may be considered that the main body is approximately in the dimensions claimed when compared to much larger devices.

Regarding claim 4, the reference teaches that the memory unit may be a flash memory.

Regarding claim 5, the reference discloses an adapter device 10 adapted to be loaded in host equipment comprising a substantially rectangular main body unit 16, a first set of connection terminals 22 provided at one end of said main body unit to enable electrical connection between said main body unit and the host equipment, a plurality loading sections 28 provided in said main body unit, each of said loading sections having an insertion opening along an edge of said main body unit transverse to said one end and a second set of connection terminals 20 spaced from said insertion opening, a plurality of substantially rectangular integrated chips 12 assembled in respective ones of said loading sections, each of said integrated circuit chips including a built-in integrated circuit unit forming a memory unit in electrical connection with said second set of connection terminals in said loading section, a guide support provided in each of said loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of said integrated circuit chips into said loading sections and a controller disposed in said main body unit for controlling the integrated circuit chips loaded in said loading sections.

Regarding claim 6, the reference discloses a substantially rectangular integrated circuit chip 12 adapted to be loaded in an adaptor device 10 for use in

host equipment, said integrated circuit chip comprising a main body unit removably insertable into the adaptor device, an integrated circuit unit disposed in said main body unit, a set of terminals 14 provided at one end of said main body for establishing an electrical connection enabling information signals to be exchanged between said integrated circuit unit and the adaptor device, a guide support unit provided on a side of said main body unit for guiding the insertion of said main body unit into the adaptor device.

Regarding claim 7, the reference discloses that said integrated circuit chip may be a flash memory.

Regarding claim 8, the integrated circuit chip may be a logic circuit unit.

3. Claim 9 is rejected under 35 U.S.C. 102(e) as being anticipated by Fan (US 6,665,736). Regarding claim 1, the reference discloses a substantially rectangular dummy chip 501adapted to be loaded in an adaptor device 500 for use in host equipment comprising a main body unit removably insertable into the adaptor device and a guide support unit provided on a side of said main body unit for guiding the insertion of said main body unit into or removal of said main body unit from the adaptor device.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong T. Vu whose telephone number is (571) 272-2111. The examiner can normally be reached on Mon. & Tues., 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David S. Martin can be reached on (571) 272-2107. The

fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PTVu
Patent Examiner